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PATENT NUMBER and
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6515910

U.S. UTILITY Patent Application

APPL NUM 10076826	FILING DATE 02/15/2002	CLASS 365	SUBCLASS 145.22	GAU 2818	EXAMINER HOANG, HUAN
**APPLICANTS: Lee Peter; Tsao Hsing-Ya; Tran Tam; Hsu Fu-Chang;					
**CONTINUING DATA VERIFIED: <i>10/076826</i> THIS APPLN CLAIMS BENEFIT OF 60/273,585 03/06/2001					
** FOREIGN APPLICATIONS VERIFIED: <i>10/076826</i>					
PG-PUB	DO NOT PUBLISH <input checked="" type="checkbox"/>	RESCIND <input type="checkbox"/>		ATTORNEY DOCKET NO AP01-005	
Foreign priority claimed 35 USC 119 conditions met		<input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> yes <input checked="" type="checkbox"/> no		U.S.DEP.T. OF COMM./PAT. & TM-PTO-136L (Rev. 12-94)	
Verified and Acknowledged Examiners initials <i>HU</i>					
TITLE : Bit-by-bit Vt-correction operation for nonvolatile semiconductor one-transistor cell, nor-type flash EEPROM					

NOTICE OF ALLOWANCE MAILED <i>10/22/02</i> (0-2370)		Assistant Examiner <i>HUAN HOANG</i> PRIMARY EXAMINER Primary Examiner	CLAIMS ALLOWED	
Amount Due <i>640</i>	Date Paid <i>12-9-02</i>		Total Claims <i>25</i>	Print Claim for O.G <i>1</i>
TERMINAL <input type="checkbox"/>		DRAWING		
DISCLAIMER		Sheets Drwg. <i>15</i>	FIGS. Drwg. <i>17</i>	Print Fig. <i>7A</i>
PREPARED FOR ISSUE		<i>HAYES 10/30/02</i> Application Examiner		
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Drawing

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